

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant:** DAVID F. SKOLL et al.  
**Serial No.:** Not yet assigned.  
**Division of Serial No. 09/927,551**  
**Filed:** Concurrently herewith.  
**Title:** DESIGN ANALYSIS WORKSTATION  
FOR ANALYZING INTEGRATED  
CIRCUITS  
**Agent of Record:** Max R. Wood      Tel: (613) 780-8681

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Assistant Commissioner for Patents  
Washington, D.C. 20231  
U.S.A.

Sir:

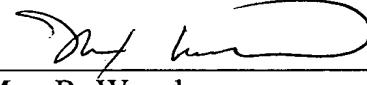
**INFORMATION DISCLOSURE STATEMENT**  
**PRIOR TO FIRST OFFICE ACTION**

Pursuant to the duty of disclosure under 37 CFR 1.56, copies of the references listed on the attached PTO Form 1449 are submitted herewith.

The Examiner is kindly requested to consider these references during the examination of the above-identified application, making the references of record, and to return an initialed copy of the PTO-1449 Form to the below-signed agent.

In accordance with 37 CFR 1.97(h), the submission of the present information is not to be construed as an admission that such information is, or is considered to be material to patentability.

Respectfully submitted,  
DAVID F. SKOLL et al.

By: 

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Encls.

Form PTO-1449 (Rev.7-80)	U.S. Department of Commerce Patent & Trademark Office	ATTY.DOCKET NO. 9-14774-1US-1-1	SERIAL NO. Not yet assigned.
LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT DAVID F. SKOLL et al.	
		FILING DATE: Concurrently herewith.	GROUP

## U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	4,623,255	18 Nov/86	Suszko	356	389	13 Oct/83
	AB	5,086,477	4 Feb/92	Yu et al.	382	8	7 Aug/90
	AC	5,191,213	2 Mar/93	Ahmed et al.	250	310	5 July/91
	AD	5,561,293	1 Oct/96	Peng et al.	250	307	20 Apr/95
	AE	5,694,481	2 Dec/97	Lam et al.	382	145	12 Apr/95
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

## FOREIGN PATENT DOCUMENTS

		Document number	Date	Country	Class	Subclass	Translation
	AL	2,216,589	26 Sep/97	Canada	G06T	7/00	
	AM	2,216,900	26 Sep/97	Canada	G06T	7/60	
	AN						
	AO						
	AP						

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

AR	Article: "Chip Scanner System High Resolution SEM Image Capture and conversion from image to GDS-11 layout, George Lanzarotta, Raith USA, Inc., November 1999
AS	Article" "Computer-Aided Reconstruction of IC Layout from Image-Based Representation" C.C. Jong et al., Sept. 1993, Proceedings of the 5 <sup>th</sup> International Symposium on IC Technology, Systems ADN Applications, Nanyang Technological University, Singapore.
AS	Article: "Integrated Circuit Chip Layer Analysis", Tan Ooi Kiang et al., Sept. 1993, Proceedings of the 5 <sup>th</sup> International Symposium on IC Technology, System and Applications, Nanyang Technological University, Singapore.

Examiner	Date considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	